x1149 Boundary Scan Analyzer

Maximize your efficiency with the versatile Keysight x1149

Introduction

The Keysight x1149 is a comprehensive and versatile board test solution that provides everything you need to efficiently test and analyze circuit boards during every stage of the development process. Whether in the research and development phase or preparing for production, the Keysight x1149 makes it easy to design, analyze, and test your circuit boards with its coherent software interface.

KEYSIGHT

Overview

The Keysight x1149 is an essential tool for engineers and technicians looking to perform highly accurate and comprehensive structural tests on their Printed Circuit Board Assemblies (PCBAs). Its advanced capabilities allow you to easily perform essential tests such as open and short tests, ensuring that your PCBAs are free from defects and functioning well.

In addition to structural testing, it also offers In-System Programming for various devices, such as Field-Programmable Gate Arrays (FPGAs) and Complex Programmable Logic Devices (CPLDs). The x1149 allows you to program and reprogram these devices in-system, providing greater flexibility and control during development. With its advanced testing capabilities and user-friendly software, the Keysight x1149 is the ideal solution for all your circuit board testing needs.

The IEEE-Compliant x1149 boundary scan analyzer

The x1149 Boundary Scan Analyzer complies with the IEEE 1149.1 Standard Test Access Port (TAP), boundary scan architecture, and IEEE 1149.6-2015 Standard Testing for Advanced Digital Network. It supports the following IEEE standards.

- IEEE 1149.1-2001
- IEEE 1149.1-2013
- IEEE 1149.6-2003
- IEEE 1149.6-2015
- IEEE 1581-2011
- IEEE 1687-2014

Industries and applications

The x1149 Boundary Scan Analyzer is purposefully engineered to cater to diverse industries and applications, addressing a broad spectrum of testing requirements, including but not limited to:

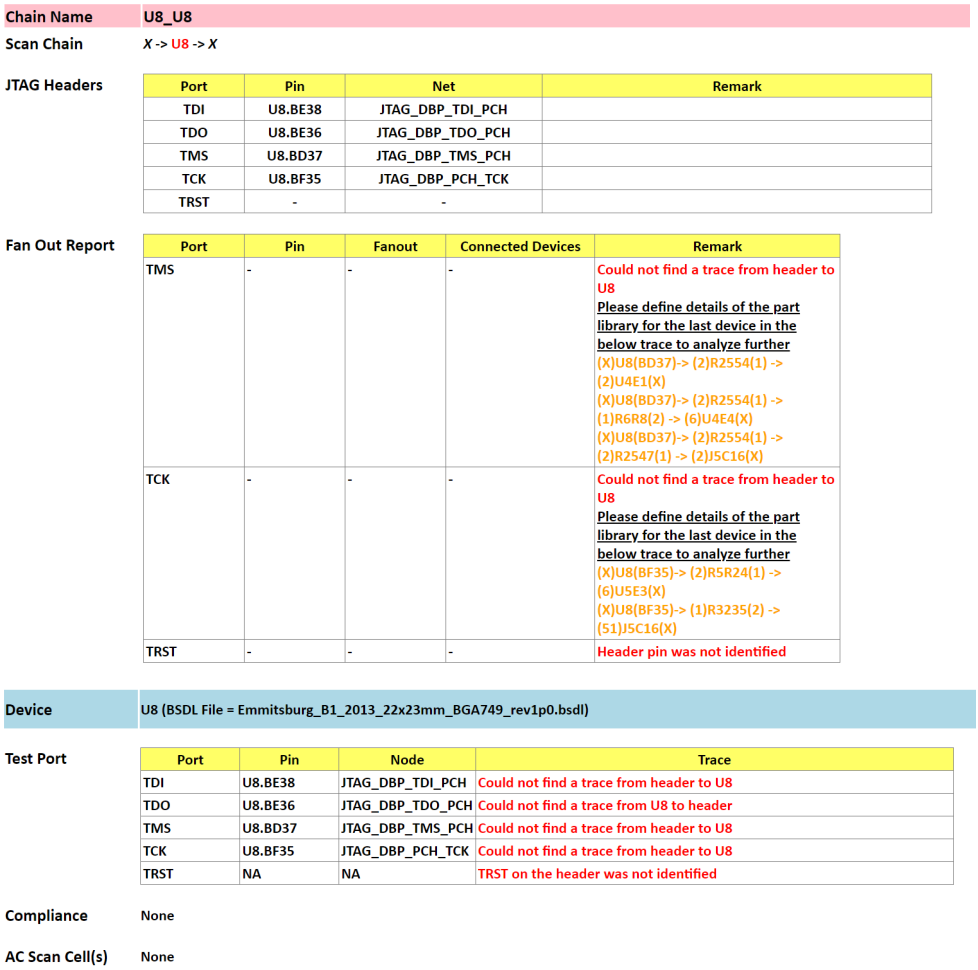
- Computational and server board test
- Network communication board test
- Aerospace and defense
- Automotive electronics test
- Industrial electronics test
- Medical device test
- Smartphones
- Storage devices (SSD, HDD)

This versatility ensures that the x1149 is a comprehensive solution capable of meeting the unique testing demands across various sectors.

DFT Analyzer

The built-in DFT Analyzer in the Keysight x1149 Boundary Scan Analyzer provides valuable insights into the design of your boundary-scan chain topology. With its advanced capabilities, the DFT Analyzer can accurately evaluate the integrity of the boundary-scan chain, identifying potential issues such as broken connections or fan-out problems. This enables you to address any issues before they become significant challenges, ultimately reducing the time and effort required to develop test programs.

With the DFT Analyzer, you are assured of the validity of your boundary-scan chain, ensuring that your testing is efficient and effective. This feature is handy for industry professionals in aerospace and defense, automotive electronics, industrial electronics, and medical device testing, where accuracy and efficiency are essential.



Chain Name	U8_U8
Scan Chain	*X* -> U8 -> *X*

JTAG Headers

Port	Pin	Net	Remark
TDI	U8.BE38	JTAG_DBP_TDI_PCH	
TDO	U8.BE36	JTAG_DBP_TDO_PCH	
TMS	U8.BD37	JTAG_DBP_TMS_PCH	
TCK	U8.BF35	JTAG_DBP_PCH_TCK	
TRST	-	-	

Fan Out Report

Port	Pin	Fanout	Connected Devices	Remark
TMS	-	-	-	Could not find a trace from header to U8 Please define details of the part library for the last device in the below trace to analyze further (X)U8(BD37)-> (2)R2554(1) -> (2)U4E1(X) (X)U8(BD37)-> (2)R2554(1) -> (1)R6R8(2) -> (6)U4E4(X) (X)U8(BD37)-> (2)R2554(1) -> (2)R2547(1) -> (2)J5C16(X)
TCK	-	-	-	Could not find a trace from header to U8 Please define details of the part library for the last device in the below trace to analyze further (X)U8(BF35)-> (2)R5R24(1) -> (6)U5E3(X) (X)U8(BF35)-> (1)R3235(2) -> (51)J5C16(X)
TRST	-	-	-	Header pin was not identified

Device	U8 (BSDL File = Emmitsburg_B1_2013_22x23mm_BGA749_rev1p0.bsdl)

Test Port

Port	Pin	Node	Trace
TDI	U8.BE38	JTAG_DBP_TDI_PCH	Could not find a trace from header to U8
TDO	U8.BE36	JTAG_DBP_TDO_PCH	Could not find a trace from U8 to header
TMS	U8.BD37	JTAG_DBP_TMS_PCH	Could not find a trace from header to U8
TCK	U8.BF35	JTAG_DBP_PCH_TCK	Could not find a trace from header to U8
TRST	NA	NA	TRST on the header was not identified

Compliance	None
AC Scan Cell(s)	None

Figure 1. DFT report

Comprehensive Range of Test Types

The Keysight x1149 Boundary Scan Analyzer has a range of test types designed to increase your fault detection coverage and simplify the debugging process. These test types are carefully selected to provide comprehensive coverage of your circuit board, enabling you to identify and resolve any issues that may arise quickly.

Whether you're working with computational or server boards, network communication boards, or other electronics applications, the Keysight x1149 provides the tools you need to perform in-depth and effective testing. The built-in test types help you identify challenges earlier in the development process, reducing the time and effort required for your product to go to market. With the Keysight x1149, you can be assured of the reliability and performance of your printed circuit board, knowing that you've taken the necessary steps to ensure its quality and reliability.

New BSDL Format

IEEE 1149.1-2013 and 1149.6-2015

The new Keysight x1149 2.1 has a new BSDL format that seamlessly supports both IEEE 1149.1-2013 and 1149.6-2015 standards. With this advancement, you can experience enhanced boundary scan testing capabilities, providing improved test coverage, streamlined debugging, and efficient fault detection. Integrating these standards empowers you to confidently tackle complex digital systems and high-speed interfaces while benefiting from accurate test pattern generation and seamless integration.

```
use STD_1149_1_2013.all;
use STD_1149_6_2015.all;

attribute COMPONENT_CONFORMANCE of ebg_a0 : entity is "STD_1149_1_2013";

attribute PIN_MAP of ebg_a0 : entity is PHYSICAL_PIN_MAP;
```

Figure 2. New BSDL format that supports IEEE1149.1-2013 and IEEE1149.6-2015

Segmented Boundary Scan Register

This innovation empowers you to effortlessly toggle the activation of specific segments from the x1149 software GUI, granting you unparalleled control for focused and precise debugging. By strategically excluding segments from the test sequence, you can experience a substantial reduction in overall test time, resulting in a more streamlined testing process.

Additionally, the power to toggle power domain segments on and off delivers direct governance over power access to corresponding segments—aligning perfectly with the definitions in your component's BSDL.

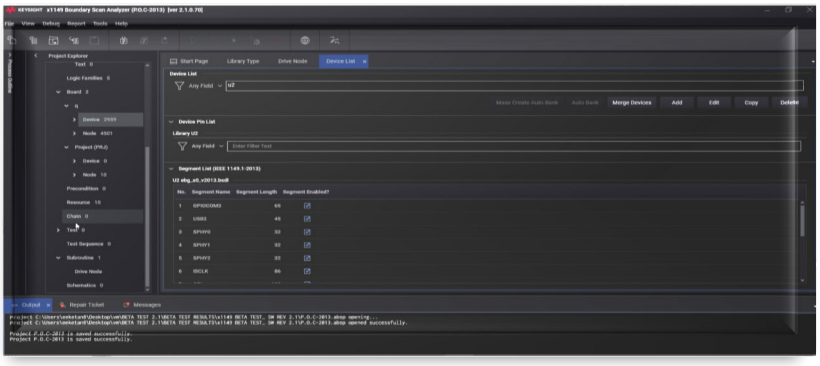


Figure 3. The x1149 software empowers users to effortlessly toggle specific segments on or off, enhancing testing precision and efficiency.

Component Initialization

Initiate seamless testing with the Component Initialization feature. By employing the initialization instruction prior to the Boundary Scan Test, the chip seamlessly enters JTAG mode for testing. In this version, the initialization instruction (Init_data, Init_status register, Init_Setup, Init_Clamp, Init_Run) guides the function, simplifying the pre-test setup process and ensuring an efficient transition into the test mode.

Register Mnemonics

Register mnemonics provide meaningful test names for values loaded into a TDR. These mnemonics bridge the gap between machine- and human-readable BSDL descriptions of the test logic, improving post-design test value setup. This functionality proves invaluable long after IC designers have progressed, significantly reducing errors and expediting test development.

```
attribute REGISTER_MNEMONICS of SERDES : package is
   "SerDes_Protocol  (off    (0b000) <I/Os powered down>, "&
      "               SATA   (0b010) <SATA>, "&
      "               SRIO   (0b011) <Serial RapidIO>, "&
      "               XAUI   (0b100) <XAUI>, "&
      "               Rsvd1  (0b101) <Undefined, do not use>, "&
      "               Rsvd2  (0b11X) <Undefined, do not use>),"&
   "SerDesClkSettings(F125Mhz  (0b00111), "&
      "               F100Mhz  (0b10101), "&
      "               Invalid (Others) <Do not use!>),"&
   "OnOff            (ON (1), OFF (0))";
attribute REGISTER_FIELDS of SERDES : package is
   "serdes_init [8] ( "&
      "(Protocol [3] IS (2 DOWNTO 0) DEFAULT(SerDes_Protocol(off)) ), " &
      "(CHClock [5]  IS (7 DOWNTO 3) SAFE(SerDesClkSettings(F125MHz)))" &
   "serdes_bist [4] ( "&
      "(Local_Loopback [1] IS (3) DEFAULT(OnOff(ON))  ), " &
      "(BER_en         [1] IS (2) DEFAULT(OnOff(OFF)) ), " &
      "(GoDone         [1] IS (1) DEFAULT(OnOff(OFF)) ), " &
      "(Pass           [1] IS (0)) )";
```

Figure 4. An example of the register mnemonic attribute in the BSDL file. SATA is one of the mnemonics representing the bit ‘0b0101’ group.

Electronic Chip Identification (ECID)

The ECID ensures the uniqueness of each component by assigning an exclusive value and capturing a rich history of manufacturing, testing, and usage data. The ECID code, seamlessly loaded into the ECID register in response to ECIDCODE instructions, unlocks an individualized identifier for every component, presented in a clear serial binary form. This transformative capability revolutionizes tracking across the lifecycle, leading to enhanced quality control, optimized diagnostics, and robust lifecycle management.

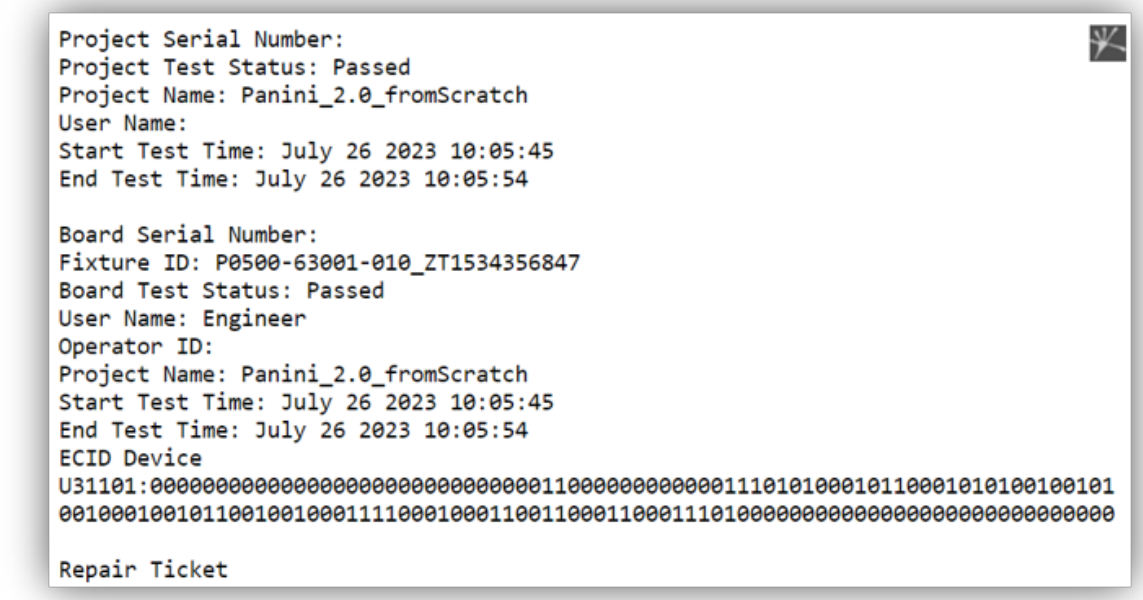


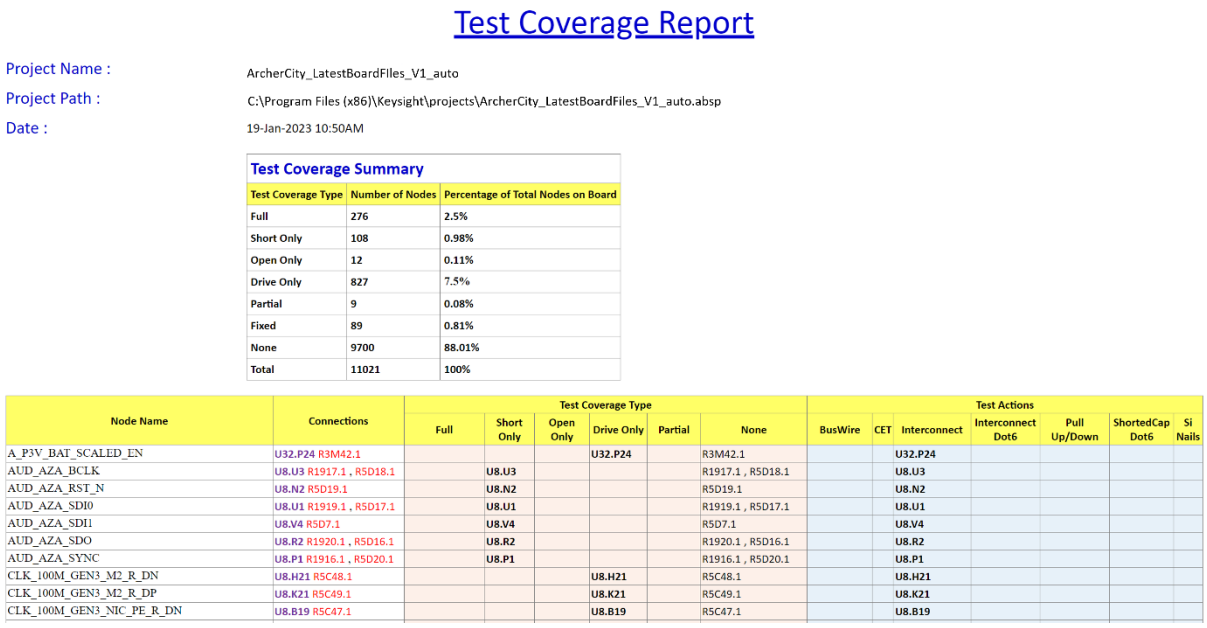
Figure 5. An example of a device with the ECID binary value which indicates the tracking information.

Effective Test Reports

Test coverage report

The built-in Design for Testability (DFT) Analyzer evaluates the Boundary Scan Chain topology design. It points out broken connections or fan-out issues to ensure the validity of the Boundary Scan chain to enable faster test program development.

- Reflects the test coverage of a project through the generated Test list
- Offers test coverage reports in various formats such as CSV, HTML, and XML
- Clearly defines test coverage classification as shown below:



Test Coverage Report

Project Name : ArcherCity_LatestBoardFiles_V1_auto

Project Path : C:\Program Files (x86)\Keysight\projects\ArcherCity_LatestBoardFiles_V1_auto.absp

Date : 19-Jan-2023 10:50AM

Test Coverage Summary

Test Coverage Type	Number of Nodes	Percentage of Total Nodes on Board
Full	276	2.5%
Short Only	108	0.98%
Open Only	12	0.11%
Drive Only	827	7.5%
Partial	9	0.08%
Fixed	89	0.81%
None	9700	88.01%
Total	11021	100%

Node Name	Connections	Test Coverage Type						Test Actions						
		Full	Short Only	Open Only	Drive Only	Partial	None	BusWire	CET	Interconnect	Interconnect Dot6	Pull Up/Down	ShortedCap Dot6	Si Nails
A_P3V_BAT_SCALED_EN	U32.P24 R3M42.1				U32.P24		R3M42.1			U32.P24				
AUD_AZA_BCLK	U8.U3 R1917.1 , R5D18.1		U8.U3				R1917.1 , R5D18.1			U8.U3				
AUD_AZA_RST_N	U8.N2 R5D19.1		U8.N2				R5D19.1			U8.N2				
AUD_AZA_SDI0	U8.U1 R1919.1 , R5D17.1		U8.U1				R1919.1 , R5D17.1			U8.U1				
AUD_AZA_SDI1	U8.V4 R5D7.1		U8.V4				R5D7.1			U8.V4				
AUD_AZA_SDO	U8.R2 R1920.1 , R5D16.1		U8.R2				R1920.1 , R5D16.1			U8.R2				
AUD_AZA_SYNC	U8.P1 R1916.1 , R5D20.1		U8.P1				R1916.1 , R5D20.1			U8.P1				
CLK_100M_GEN3_M2_R_DN	U8.H21 R5C48.1				U8.H21		R5C48.1			U8.H21				
CLK_100M_GEN3_M2_R_DP	U8.K21 R5C49.1				U8.K21		R5C49.1			U8.K21				
CLK_100M_GEN3_NIC_PE_R_DN	U8.B19 R5C47.1				U8.B19		R5C47.1			U8.B19				

Figure 6. Test coverage report for test coverage classification

Test Point Reduction (TPR) report

One distinct feature of the Keysight x1149 is that it can produce a test point reduction report, showcasing its test coverage of the x1149 test. You can leverage this report to optimize the test points needed on the board. With the TRP report, it will help you in:

- Reducing tester resources which results in lower fixture costs
- Reducing engineering effort on test debug
- Reducing test point real estate on a dense PCB

```
!-------------------------------------------------------------------------------------------------------------------------------
! TEST POINT REDUCTION LIST
! Project Name                          : C:\Project Files (x86)\Keysight\projects\ArcherCity_LatestBoardFiles_V1_auto.absp
! Date Generated                        : 19-Jan-2023 10:53AM
! Total No. of Nodes Needing Test Points : 10526
! Total No. of Nodes Tested             : 495
! Total No. of Nodes on Board           : 11021
! Node Coverage Categories include      : Full         146     (1.32%)
!                                         Short Only   19      (0.17%)
!                                         Open Only    0       (0.00%)
!                                         Drive Only   0       (0.00%)
!                                         Partial      330     (2.99%)
!                                         None         10526   (95.51%)
!-------------------------------------------------------------------------------------------------------------------------------

!-----------------------------------------------------------------------------------------
! NODE NAME:  CONNECTIONS:  TESTED BY
!-----------------------------------------------------------------------------------------

!Nodes with all "Full" test coverage pins
CLK_24M_66M_LPC0_ESPI_BMC : U32.AE7, R7B42.2 : Interconnect, Bus Wire
CLK_25M_OSC_DEBUG_FPGA : U8C1.V9, R7C43.2 : Bus Wire, Interconnect
CLK_25M_OSC_MAIN_FPGA : U31.P11, R7C42.2 : Bus Wire, Interconnect
ESPI_IO0_LPC_LAD0_PCH : U8.BG12, R4018.1 : Interconnect, Resistor Pull Up/Down, Bus Wire
ESPI_IO0_LPC_LAD0_R : U32.AB7, R7B45.2 : Interconnect, Resistor Pull Up/Down, Bus Wire
ESPI_IO1_LPC_LAD1_PCH : U8.BF19, R4017.1 : Interconnect, Bus Wire
ESPI_IO1_LPC_LAD1_R : U32.AB8, R3M30.2 : Interconnect, Bus Wire
ESPI_IO2_LPC_LAD2_PCH : U8.BE18, R4016.1 : Interconnect, Bus Wire
ESPI_IO2_LPC_LAD2_R : U32.AC8, R7B43.2 : Interconnect, Bus Wire
ESPI_IO3_LPC_LAD3_PCH : U8.BD19, R4015.1 : Interconnect, Bus Wire
ESPI_IO3_LPC_LAD3_R : U32.AC7, R7B44.2 : Interconnect, Bus Wire
FM_ADR_ACK_R : U31.F19, R6E34.2 : Interconnect, Bus Wire
FM_ADR_MODE0 : U31.F18, R6E53.2 : Interconnect, Bus Wire
FM_ADR_MODE1 : U31.F22, R6E41.1 : Interconnect, Bus Wire
FM_ADR_TRIGGER_R_N : U8.AH4, R4R21.1 : Interconnect, Bus Wire
FM_BIOS_POST_CMPLT_BMC_N : U32.AC9, R3M15.2 : Interconnect, Bus Wire
FM_BMC_CRASHLOG_TRIG_N : U31.D17, U32.H23 : Interconnect, Bus Wire
```

Figure 7. An example of a TRP report

Autobank

Improving the speed and efficiency of memory testing

The Autobank feature is a powerful tool that allows for parallel testing of multiple memories. This innovative feature significantly improves the speed and efficiency of memory testing, enabling you to perform comprehensive tests in less time. By testing multiple memories simultaneously, you can quickly identify any faults or issues and take action to resolve them before they become major problems. The Autobank feature saves valuable time and resources, allowing you to focus on other critical tasks.

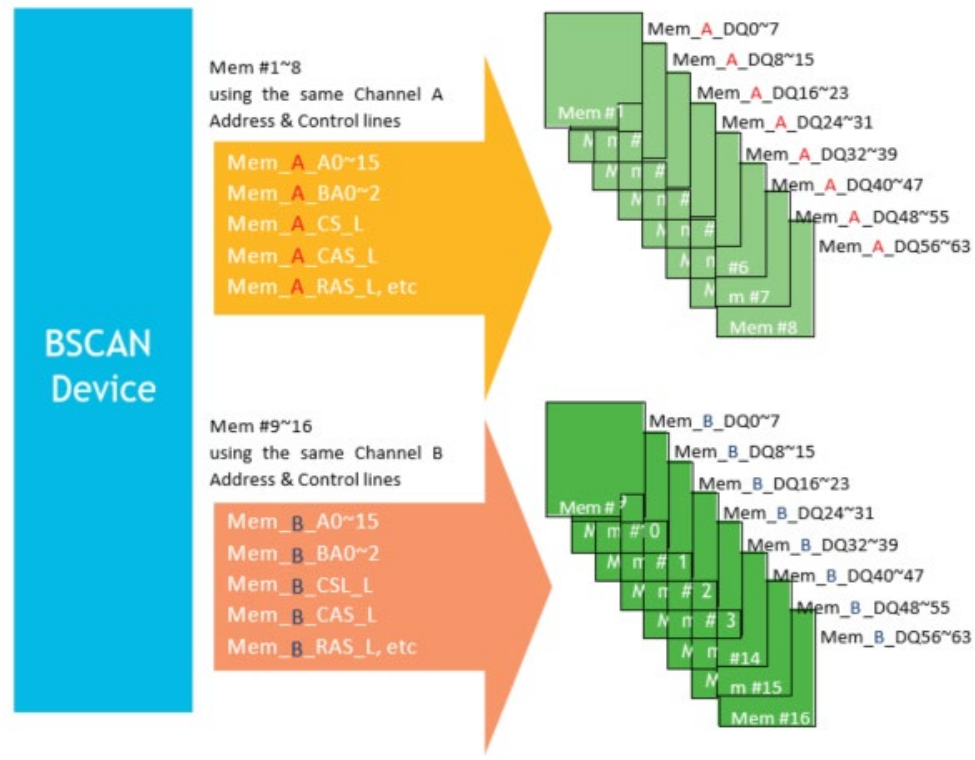


Figure 8. Multiple memories test in parallel with Autobank

CET Cover-Extend Technology (CET)

Maximize test coverage on connectors and non-boundary scan devices

CET Cover-Extend Technology (CET) is one of the limited test access solutions Keysight Technologies provides. Unlike VTEP, which requires a dedicated resource to supply the necessary stimulus, CET obtains its stimulus from a Boundary Scan IC that complies with the IEEE1149 standard, which lets you control the IC with just four pins (TMS, TCK, TDI, and TDO).

CET significantly reduces the need for physical test access and can be applied to both connectors and non-boundary scan components. The CET module is connected to the x1149 controller CET port through an HDMI cable, and nanoVTEP sensors are connected to the nanoVTEP amplifier board and then wired to one of the 64 ports on the MUX card in the CET module.

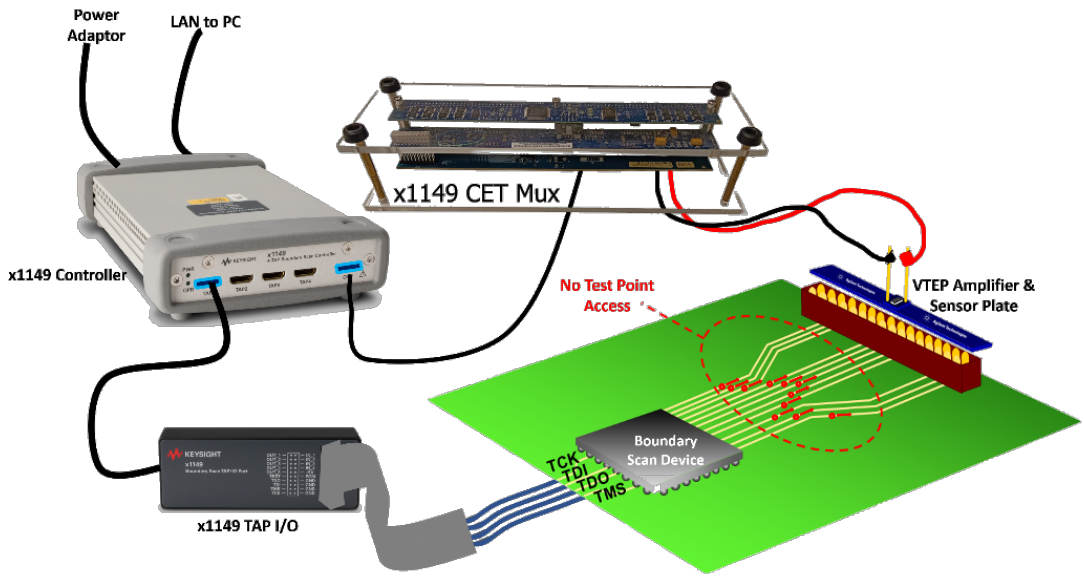


Figure 9. CET module connection diagram

Multi-Chain Generation

Effortless integration of multiple TAP boards with x1149's onboard linker

The Keysight x1149 Boundary Scan Analyzer boasts a unique onboard linker feature that simplifies the integration of multiple TAP ports. This feature enables users to daisy-chain individual chains and interconnect coverage between these chains, thus maximizing overall test coverage.

The onboard linker saves time and effort compared to conventional methods, as it eliminates the need for manual interconnections. This feature allows users to quickly and easily expand their test coverage without sacrificing accuracy. An onboard linker is a valuable tool for ensuring the complete testing of complex circuits and maximizing efficiency in the test process.

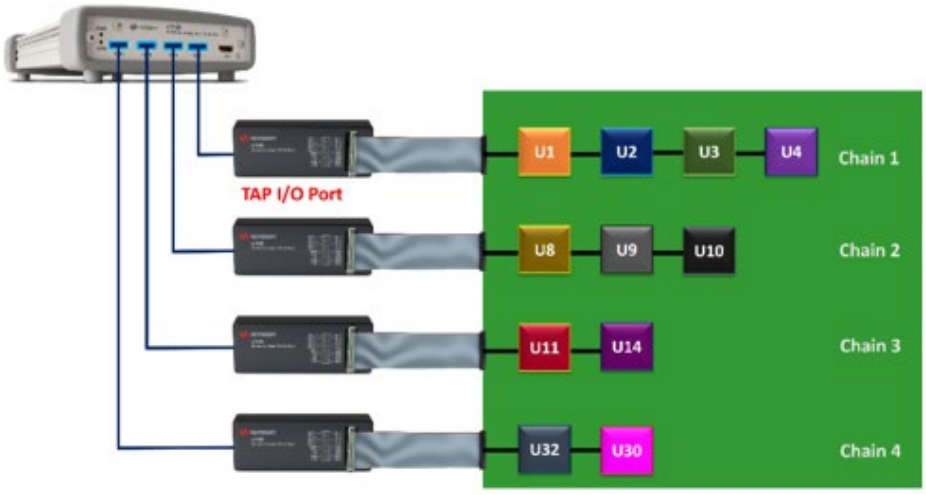


Figure 10. Independent chains: Daisy-chained to maximize test coverage

Pin Constraints

Streamline post-configured FPGA testing

The Pin Constraints feature of the Keysight x1149 Boundary Scan Analyzer offers a convenient solution for testing post-configured FPGAs. With this feature, you can remove the driver or receiver of a pin by modifying the test code, thus eliminating the need for post-configured BSDL.

Additionally, it addresses the stability issues that may arise with boundary scan cells not working on a specified node. Instead of modifying the BSDL, the Boundary Scan cell definitions on the pins can be easily altered to debug the test quickly.

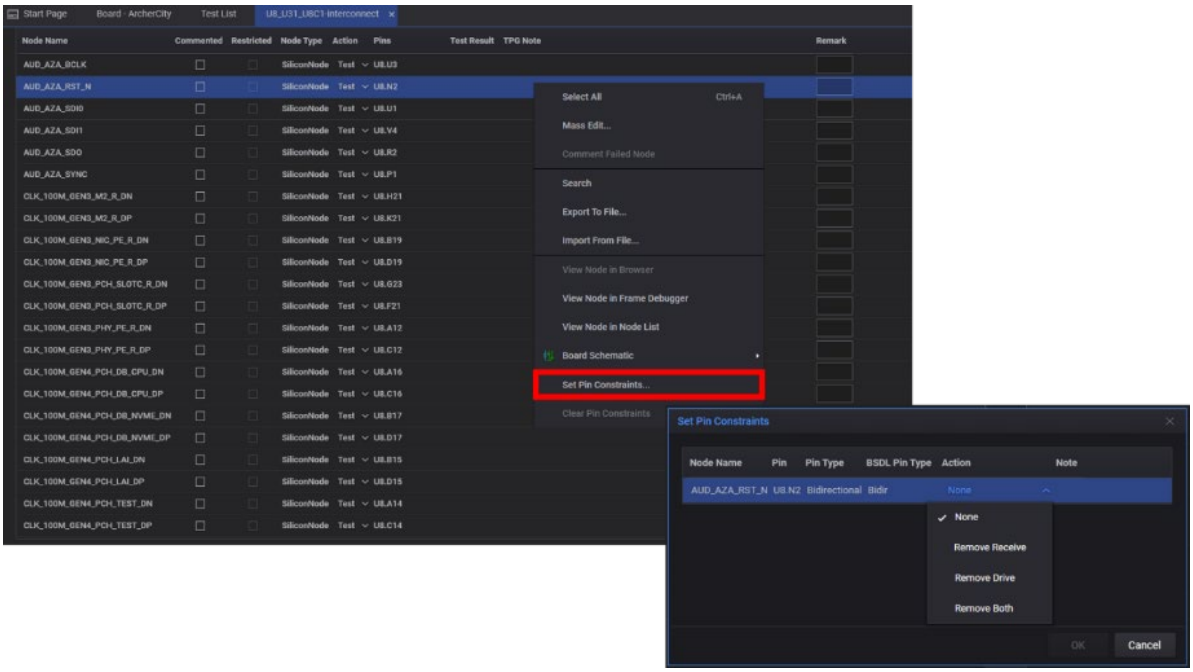


Figure 11. Setting pin constraints with the Keysight x1149 Boundary Scan Analyzer

Automated Scan Path Linker Configuration

Automated scan path linker configuration simplifies your settings by automatically configuring the parameters for the selected scan path linker device. The Keysight x1149 supports the following Scan Path Linkers:

- Texas Instrument - Scansta 112
- Lattice BSCAN FPGA
- Firecron JTX05, JTX07, JTX09

By mapping the Device Designator to the scan path linker type from the 'Onboard Linker' (OBL) dropdown menu, the project configures the scan chain port mapping to this particular scan path linker device.

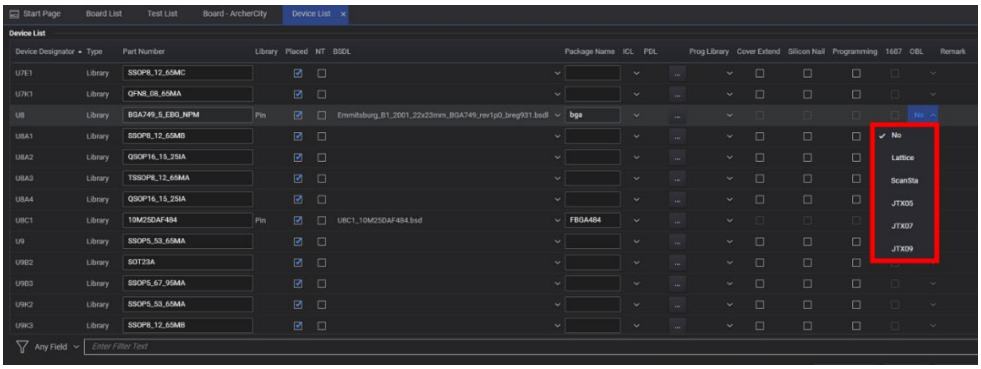


Figure 12. Automated scan path linker configuration

IEEE 1687-2014 Standards

Keysight x1149 Boundary Scan Analyzer supports IEEE 1687-2014 standards to access and control embedded instruments within a semiconductor chip. This standard provides a framework for accessing various test and debug features embedded within chips, including components like embedded instruments, built-in self-test (BIST) structures, and other on-chip resources. The IEEE1687-2014 introduces hierarchical control, enabling organized and systematic instrument access. The standard facilitates dynamic reconfiguration, allowing on-the-fly adjustments of embedded resources, even during runtime. This approach aims to reduce test time, enhance debugging capabilities, and promote interoperability among tools and devices.

With the ability to access and control embedded instruments, you can test and debug complex semiconductor chips with greater ease and efficiency.

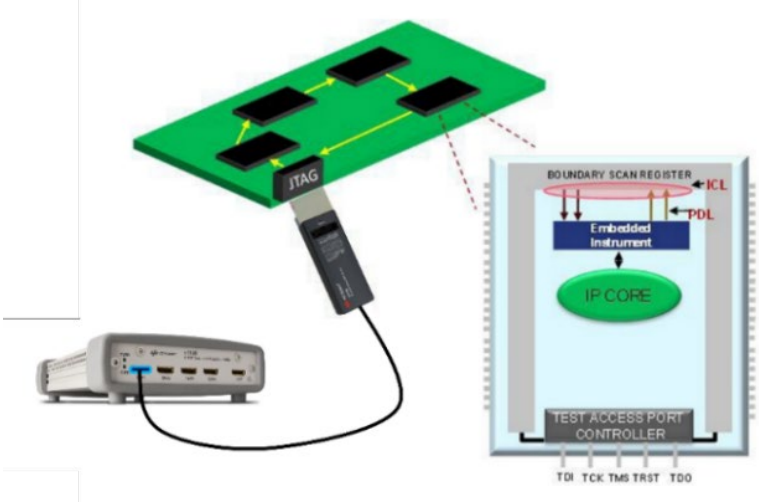


Figure 13. Access and control embedded instruments within a semiconductor chip with IEEE 1687-2014 standards.

Debugging Tools

The Keysight x1149 is equipped with a comprehensive array of advanced debugging tools to empower your testing endeavors. Notably, the Auto-Adjust tool takes center stage, effortlessly fine-tuning crucial parameters, including slew rates, TCK speed, and voltage offsets for TDI/TDO. This intelligent feature autonomously seeks the optimal configuration tailored to your unit under test (UUT), underlining the sophistication and efficiency embedded within the Keysight x1149.

Figure 14. Tweak various parameters with the Auto-adjust tool

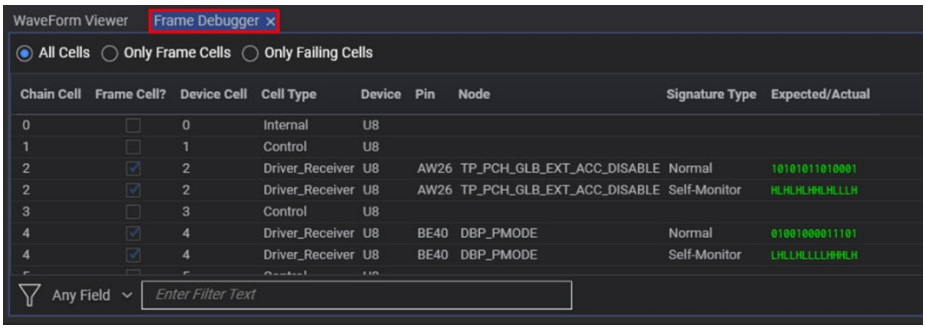


Figure 15. The frame debugger lets you perform a deep dive.

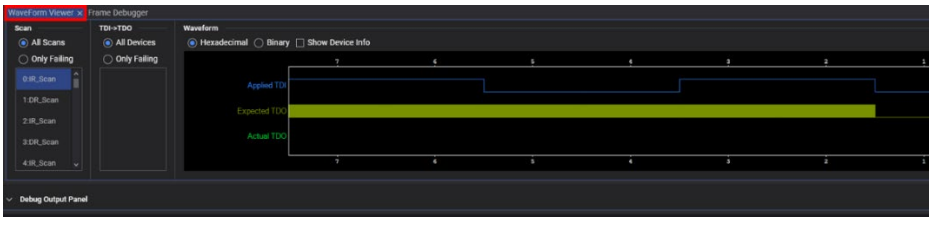


Figure 16. Waveform viewer shows the expected and actual values of the TDO signal for the test.

Insert Source Language and Custom Test

Insert Source Language (ISL) is a Keysight proprietary language used to develop custom tests utilizing the JTAG protocol. The ISL enables you to:

- Run Built-In Self Tests (BIST)
- Describe initialization sequences or preconditioning for chips, which could also help to adjust device characteristics to enable testing.

Improve Test Coverage with Keysight x1149 and i3070/i1000 Integration

Experience the pinnacle of testing solutions by integrating the Keysight x1149 Boundary Scan Analyzer and the In-Circuit Test powered by i3070/i1000. This dynamic fusion creates an unparalleled testing ecosystem where the strengths of both platforms harmonize to deliver comprehensive test coverage while minimizing testing duration. Seamlessly blending the advanced boundary scan testing capabilities of the Keysight x1149 with the robust in-circuit testing prowess of the i3070/i1000, this integration signifies the convergence of the best in electronic testing. With this harmonious union, your electronic devices are meticulously scrutinized and validated before release. The outcome is a holistic solution that optimizes testing scope and efficiency, unveiling the ultimate path to electronic testing and validation excellence.

For more information

For more information on i3070 system, visit:
www.keysight.com/us/en/products/in-circuit-test-systems/medalist-i3070-systems.html

For more information on i1000 system, visit:
www.keysight.com/us/en/products/in-circuit-test-systems/medalist-i1000-systems.html

Customized Test Card for Server Solution

The Keysight x1149 lets you incorporate the DDR3/DDR4/PCIE test cards to improve the test coverage of DIMM/PCIE connectors on a server board. Test cards test for the signal pins and the Power and Ground pins, constituting up to 50% of the connector's total pin count. In addition, Boundary Scan testing allows for fast test time. Also, it delivers the best coverage on DIMM/PCIE connectors with optimum test time.

Test Sequencer

Having control of your test execution goes beyond just rearranging the order of tests that you want to run. Engineers need the ability to insert decision-making branches and subroutines in addition to the usual prompts and wait times. The Keysight x1149 test sequence gives engineers more power over how they want the test execution to progress.

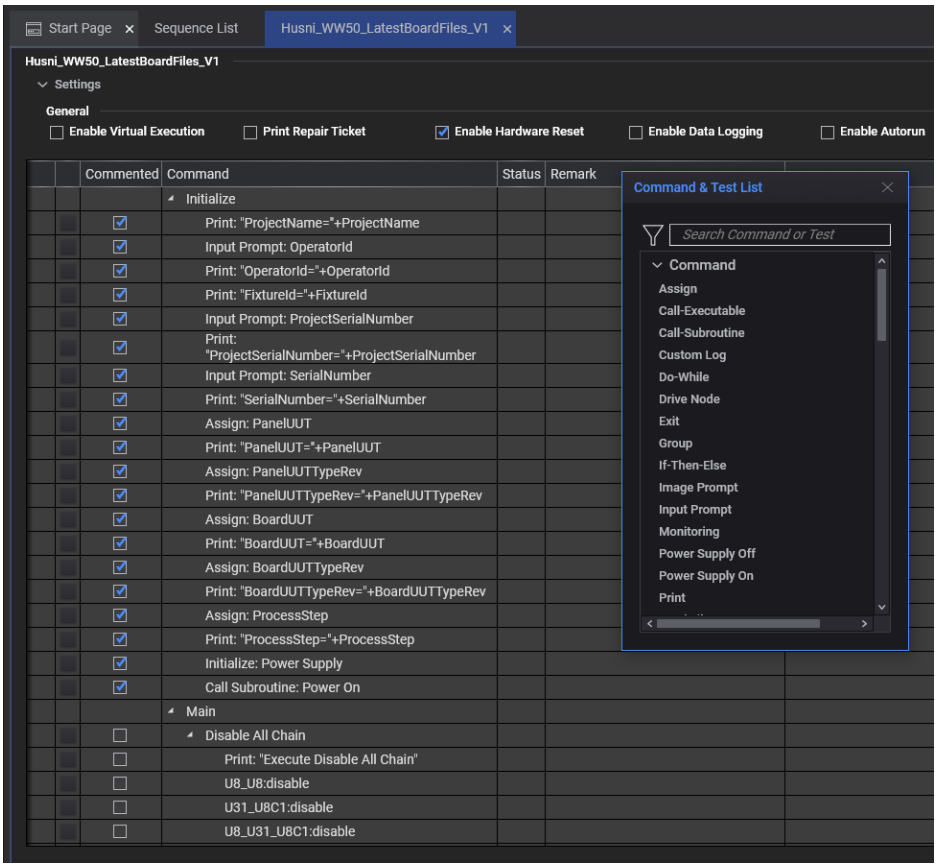


Figure 17. Rearrange the order of tests with the test sequencer

Remote Access to Controller

Work from your desk while your Keysight x1149 Boundary Scan controller sits in the lab – or even miles away. With the built-in Ethernet connection, control is just one IP address away. Unlike remote desktop control, you do not need any additional host PC or other additional hardware. Instead, you can easily connect directly to your controller.

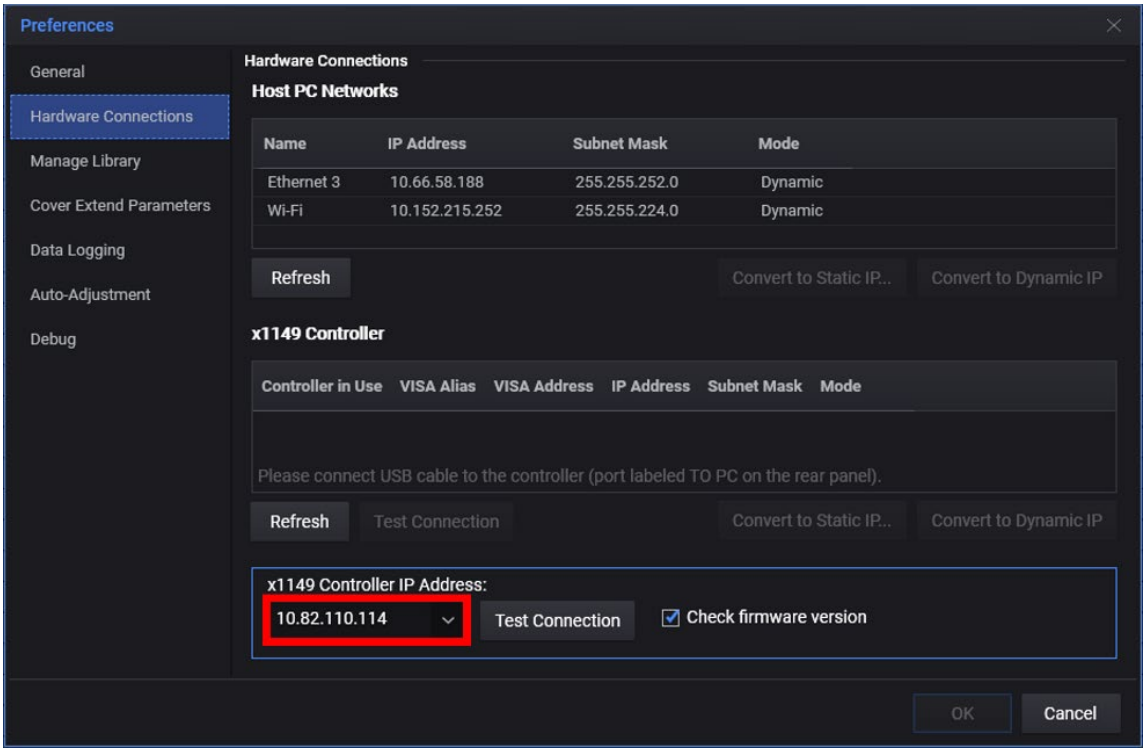


Figure 18. Setting up remote connection access that lets you connect from anywhere in the world

Dedicated TAP/IO Ports

With dedicated hardware for the Test Access Port and Digital Inputs/Outputs (TAP/IO Port), you can bring the parts that matter closer to your Unit-Under-Test (UUT) to ensure maximum signal integrity. If needed, the ports are small enough to fit into tight spots in fixtures.

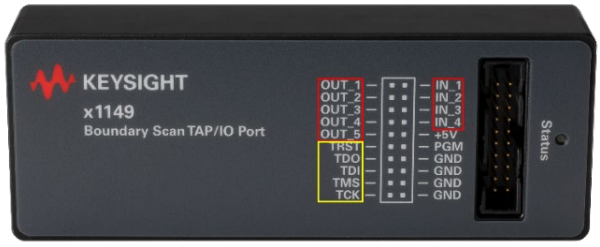


Figure 19. Dedicated TAP/OP ports

Superior Signal Quality

Signal quality is increasingly crucial as logic levels trend lower. To prevent unintended state transitions leading to false calls, you need better control of your I/Os and have them respond in the intended way. Keysight's Keysight x1149 provides excellent signal quality with low overshoots. It also gives the user the option to adjust the slew rate.

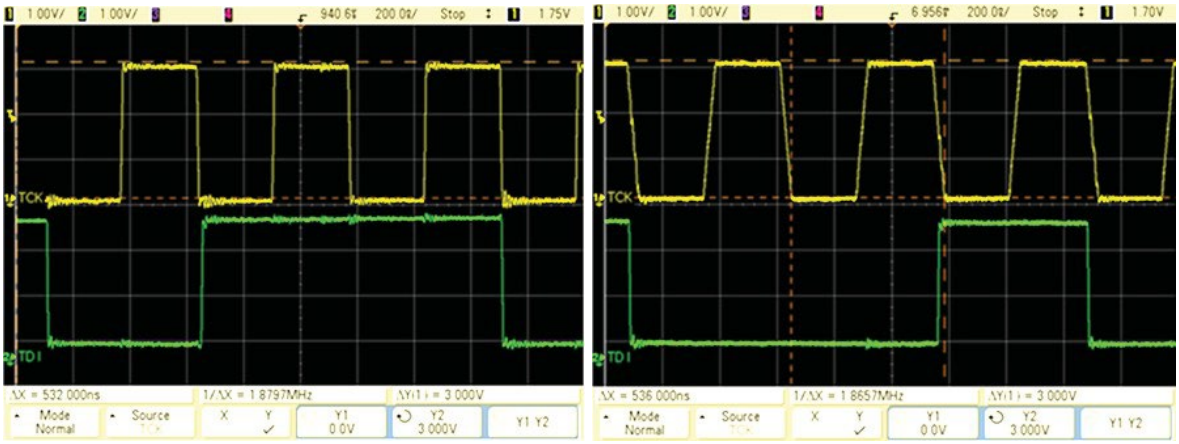


Figure 20. Excellent signal quality with low overshoots

Efficient Failure Reporting

Failure reporting is an important aspect of product testing and quality assurance. This feature enables the tracking of any failures that occur during the testing process. Utilizing failure reporting enables you to take a proactive approach to product testing and quality assurance, ensuring that your products are of the highest quality and meet customer expectations.

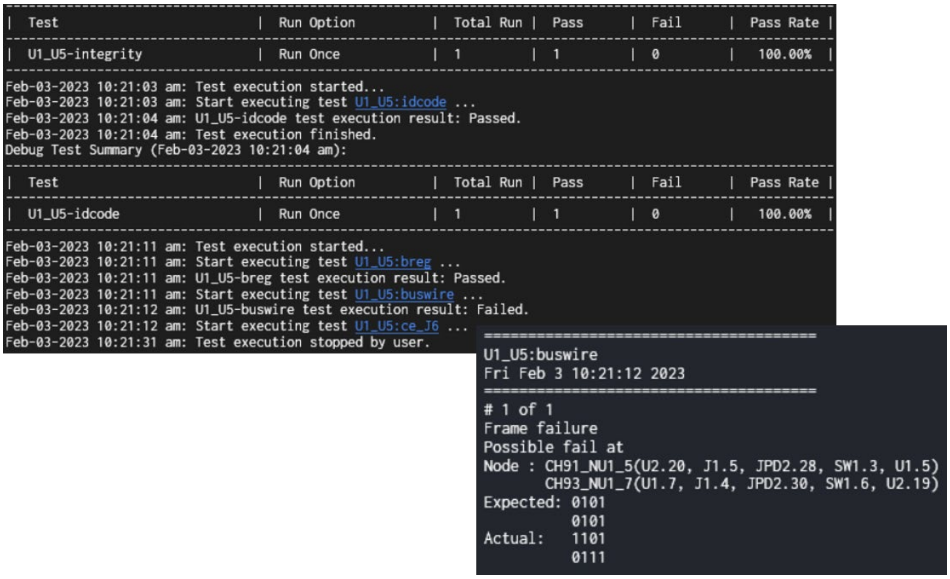


Figure 21. Failure reporting

Data logging

The Keysight x1149 software can log results during test execution. The Keysight x1149 generates a log file for every board and panel tested. You can easily save these log files in Keysight x1149 or i3070 log formats, which are user configurable. i3070 format of data logging eases integration of Keysight x1149 into shop floor systems.

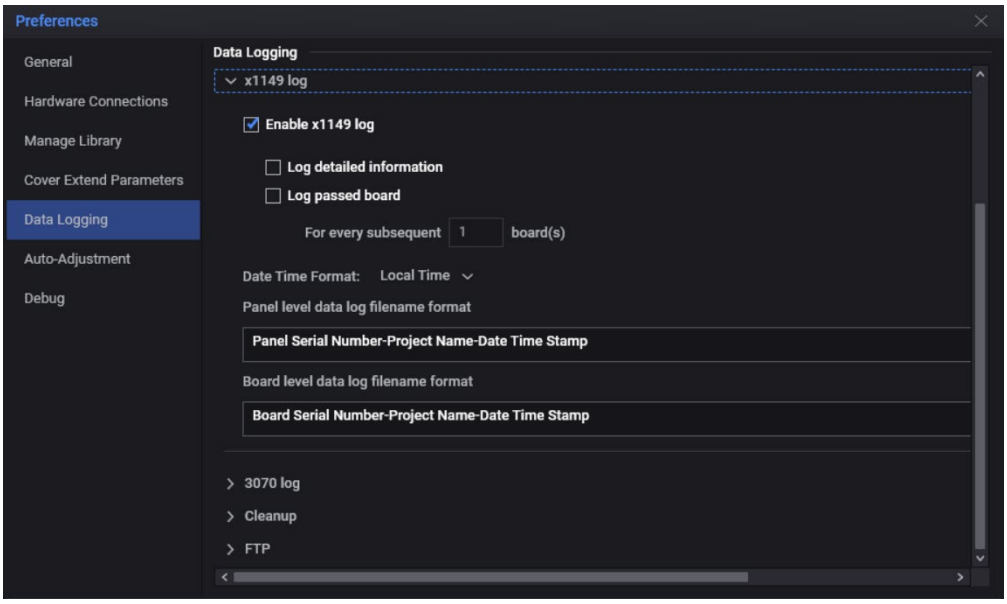


Figure 22. Configure the data logging settings the way you like

Baseline and Revision Control

Baselining allows you to track modifications in tests that have been released. Baselining is especially important during board test production runs, as it tracks and reports which tests are modified and the date when the changes were made.

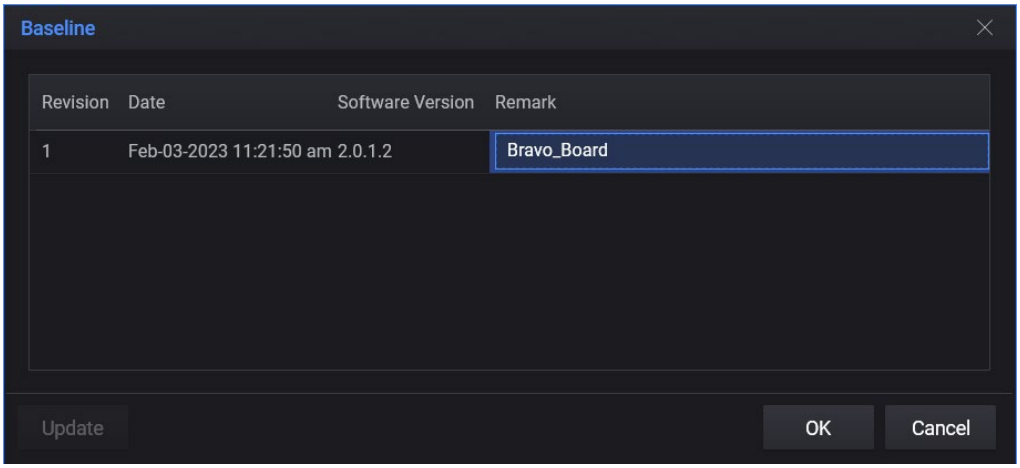


Figure 23. Baseline and revision control

Language Localization

The standard English user interface comes with a Simplified Chinese option. Our translation matrix can be modified to include additional languages. For operations spanning the globe, the ability to utilize the same software in the local language is an added advantage.

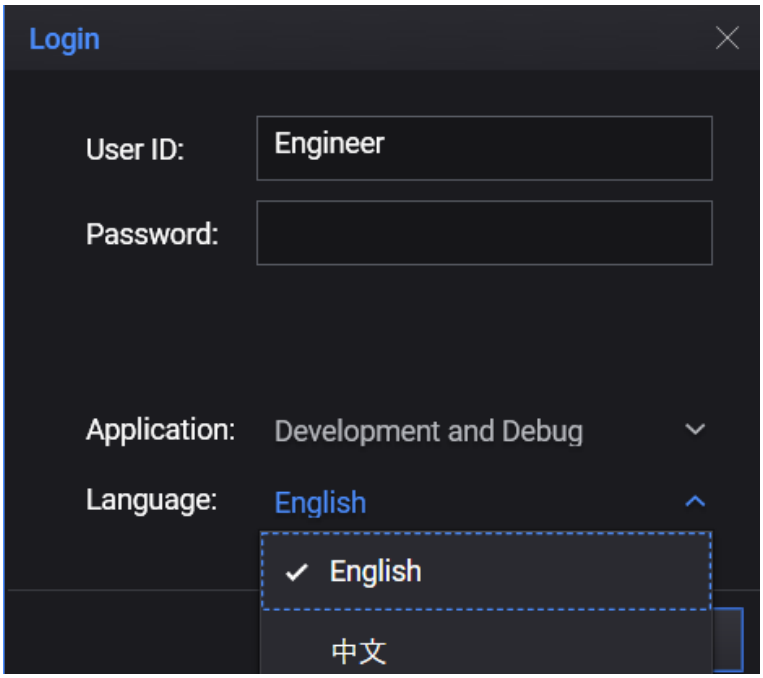
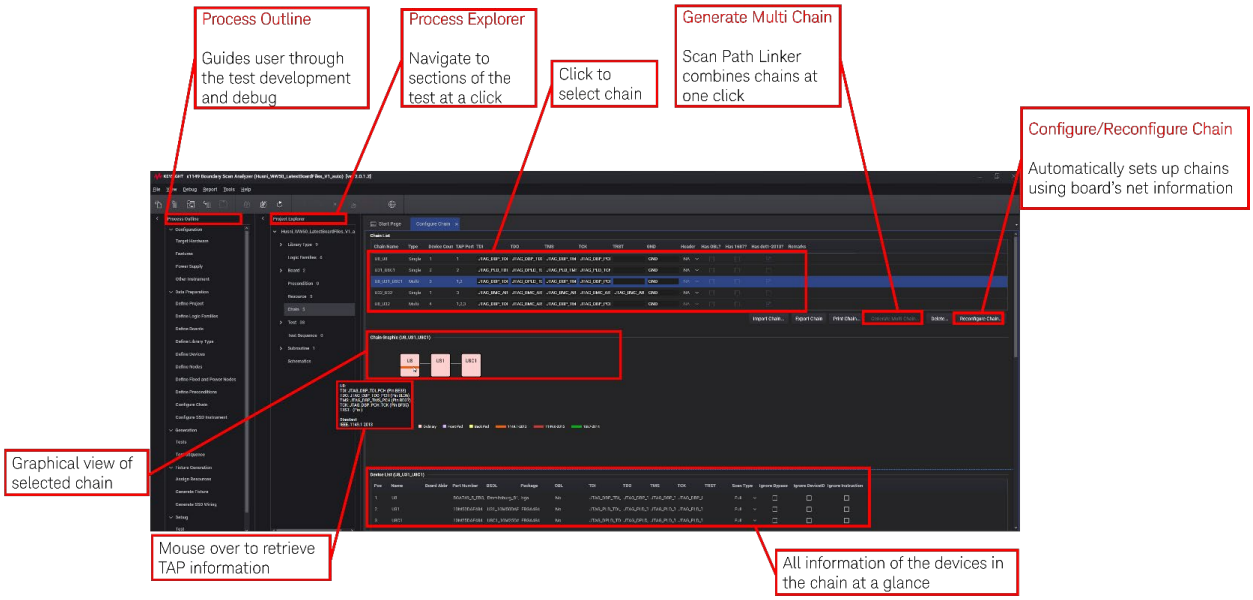
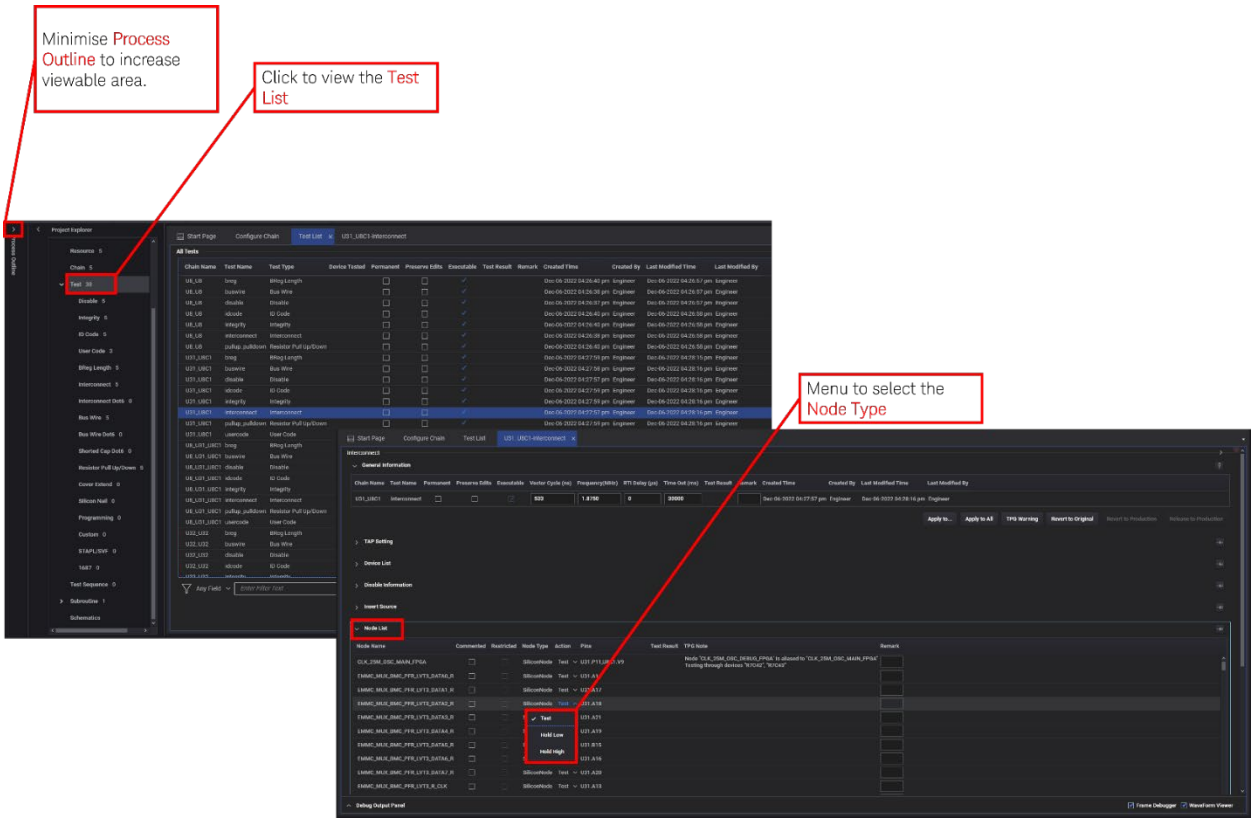
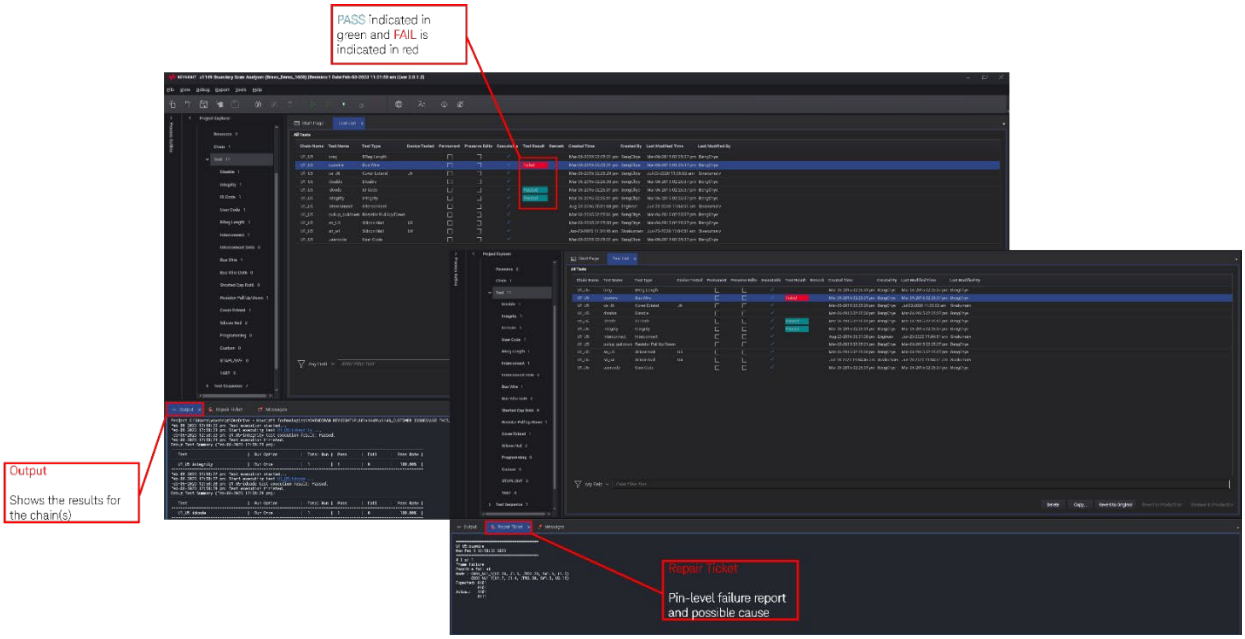


Figure 24. The x1149 software supports multiple languages

Overview of x1149 Software GUI






PASS indicated in green and FAIL is indicated in red
Output
Shows the results for the chain(s)
Repair Ticket
Pin-level failure report and possible cause

Product Characteristics and Specifications

Product characteristics

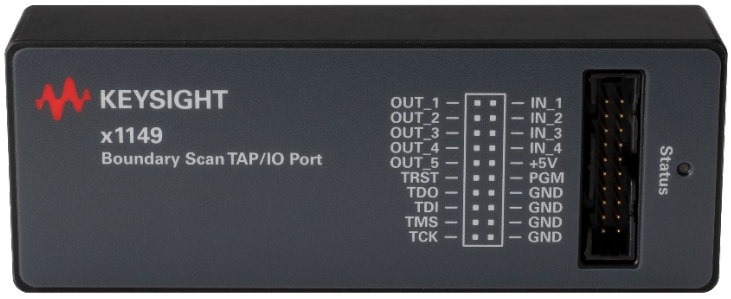
	Ethernet 10/100 MB
Controller interface	High-speed USB 2.0 (For firmware upgrade only)
Power requirement	+12 VDC (typical)
	2 A (maximum) input-rated current
	Installation category II
Power consumption	+12 VDC, 260 mA (maximum)
Standard shipped accessories	AC/DC power adapter
	Power cord
	USB cable
	HDMI cable
	Diagnostic clip
	Keysight x1149 boundary scan analyzer' Quick Start Guide.'
	Keysight x1149 software release CD-ROM
	Certificate of calibration
	* Compatible with Microsoft Windows operating systems only.
Operating environment	Operating temperature from 0 to +55 °C
	Relative humidity at 15% to 85% at 40 °C (non-condensing)
	For indoor use only
Storage compliance	–20 to 70 °C
Safety compliance	

Product dimension

Product dimension

Boundary scan controller dimension (length x width x height)	185 mm x 120 mm x 45 mm / 7.28 in x 4.72 in x 1.77 in
Weight	550 g

TAP/IO port dimension (length x width x height)	120.3 mm x 44.5 mm x 21 mm / 4.72 in x 1.75 in x 0.826 in
Weight	80 g



General specification

Parameter/specification	Driver/receiver resources
Types	GPIO, JTAG TAP
GPIO (General Purpose Input/Output)	5 output/driver pins programmable voltage and shares with the common (VREF) Voltage Reference
	4 input/receiver pins with fully programmable receiver voltage.
JTAG Test Access Port (TAP)	Supports up to 4 TAP each with TCK, TDI, TDO, and TMS with optional TRST signals as defined by IEEE Std 1149.1
	TDI, TMS, and TRST programmable voltage reference share a common VREF with the GP-output pins
	TDO programmable voltage receiver
	TCK has a separate programmable voltage reference (VREF) and slew rate.
Cover-Extend Technology (CET)	
Vectorless Enhanced (VTEP)	CET ARM, CET Rx/Tx, VTEP CLK/A/B/Hi/Lo+12 VDC Power
Ground pins	
Fixed location grounds per TAP module	TAP Module pins 1,3,5,7

Hardware GPIO (General Purpose Input/Output) Specifications

Parameter/specification	GPIO specifications
Resources	5 drivers & 4 receivers with GND pins shared with TAP Pins
Sample/update rate READ, WRITE, READ/WRITE maximum sample/update rate	10 KHz / 100 usec
Per-pin settable features	OUT: data value (0,1, or Z)
	“0” – ≤ 100 mV
	“1” – ≥ VREF-100 mV
	“Z” – High Z
	IN: VREF (1.1~5.0 V)
General purpose input or receiver	
IN/receiver	Read digital data “0” or “1”, according to VREF and threshold voltage. It can be used to measure the external voltage range from 0 V to 5 V
Reference channel group	+5 V to 0 V in 100 mV steps
Timing	De-skewed. No programmable edges
Termination	> 1 MΩ
Error detection	Windowing (two-point receive reference), over-voltage, under-voltage, drive-check validation (receiver used to verify driver achieved drive state)
General purpose output or driver	
Update rate(maximum)	10 KHz/100 µs
Output voltage [3]	Range: +5.0 V to +1.1 V, step resolution of 100 mV, static accuracy
Driver current [2]	10 mA @ 5 V
	2 mA @ 2.5 V
Continuous output current into a short [3]	50 mA at 5 V
	20 mA at 2.5 V
Rise/fall time [4]	< 20 ns @ 2.5 V
	< 50 ns @ 1.1 V
Tri-state leakage current (maximum range [5])	–65 µA,+5 µ
Tri-state capacitance (maximum):	Maximum 0.7 nF
	Typical 0.45 nF
Disconnected capacitance	15 pF
Output skew (same board)	Typical < 5 ns
DC output resistance (typical)	35 - 50 Ω

Hardware JTAG TAP specifications

Parameter/specification	Test method
JTAG TAP specifications	
Resources	TDI, TDO, TCK, TMS, TRST, and a GND pair for each 4 TAP port
Clock maximum frequency	22.5 Mhz
Per-pin settable features	Data value (0,1, or Z), driver/receive reference, slew rate; termination high-impedance or 50 Ω
Timing	De-skewed. Programmable edges (TCK only)
JTAG TAP receiver TDO	
Clock maximum frequency	11.25 Mhz
Reference voltage (thresholds)	High: +5 V
	Low: 0 V to 0.5 V
	Step resolution of 100 mV
	Static accuracy
Input voltage range	0 V to 5 V
Input resistance	> 40 KΩ
Pull-up terminations	100k Ω
JTAP TAP driver TDI, TMS, TRST	
Clock maximum frequency	TDI – 11.25 MHz
	TMS – 7.5 MHz
	TRST – 10 KHz
Output voltage	+5 V to +1.1 V 2
Driver current [3]	±10 mA @ 5 V
	±2 mA @ 2.5 V
Continuous output current into a short [3]	≥ 50 mA at 5 V
	> = 20 mA at 2.5 V
Rise/fall time [3]	< 20 ns @ 2.5 V
	< 10 nS @ 1.1 V
Tri-state leakage current (maximum [5])	±65 µA
Tri-state capacitance (maximum)	1 nF
Output skew (TMS and TRST on all TAPs) (same board)	Typical ± 5 ns
DC output resistance (typical)	35 Ω, 50 Ω

JTAP TAP Driver TCK	
Clock maximum frequency	22.5 Mhz
Output voltage [2]	0 to 5 volts with 100 mV resolution)
Driver current [3]	10 mA @ 5 V
	2 mA @ 2.5 V
Continuous output current [3]	≥ 80 mA @ 5 V
	≤ 40 mA at 2.5 V
Slew rate: (see note [6])	40 V/µsec to 380 V/µsec
Tri-state leakage current (maximum 5)	–3.7 µA
Tri-state capacitance (maximum)	1.1 nF
Disconnected capacitance	15 pF
DC output resistance (typical)	50 Ω

1. There are 4 GND pins per TAP module, which are common for both GPIO and TAP signals in the same TAP 20-pin connector. However, the GND pins in different TAP modules are isolated.
2. Vref can be configured from 1.1 V to 5.0 V with a step of 0.1 V, which is common to all GPO and TMS/TDI/TRST signals. Vref clk can be separately configured in some situations where the high voltage of TCK needs to be a little higher than the other TAP signals. The logic output high is set to a voltage range from (Vref - 0.2V) to Vref, while the logic low is less than 0.2 V when the output current is not more than 0.1 mA.
3. Capable of producing an output current of 10 mA when Vref = 5 V, or 2 mA when Vref = 2.5 V; load 100 Ω for the drive current test. The maximum current is tested when the output pin shorts to GND.
4. Rise time refers to the period when a signal rises from 0.1 Vref to 0.9V ref; fall time is the period when a signal falls from 0.9 Vref to 0.1 Vref.
5. Set the output at a high-Z state and connect the pin to GND to measure the positive leakage current; connect the pin to a maximum voltage of power reference value (Vref) for negative leakage current measurement.
6. The TCK reference voltage is set to 5 V. When the voltage for the slew rate configuration is set to 0.2 V, the reading of the TCK slew rate is ≤ 30 V/uS; while this voltage is set to 5 V, the reading is ≥ 400 V/uS.
7. The threshold voltage of TDO is normally set between 0.5 V and 3.5 V. The logic reading from TDO would be ‘1’ if the input voltage ≥ (0.1 V + threshold voltage), and ‘0’ if the input ≤ (threshold voltage – 0.1 V).

For more information

For more information on Keysight x1149 boundary scan analyzer, visit:
www.keysight.com/us/en/product/N1125A/x1149-boundary-scan-analyzer.html